Executive Summary

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1. Title of the Project:

Minimally Invasive Real-Time BCI System for Motor Neurorehabilitation Using Machine Learning Co-Processor Chip

2. Date of Start of the Project:

October 1, 2023

3. Aims and Objectives:

Motor impairment, characterized by reduced or lost motor function due to neurological conditions like stroke, cerebral palsy, Parkinson's disease, and multiple sclerosis, significantly limits physical, cognitive, and emotional quality of life. Brain-computer interfaces (BCIs) have shown promise in rehabilitating individuals with severe motor impairments through neuroplasticity, but most current BCIs rely on non-invasive methods such as EEG, which limits spatial and temporal resolution.

The aim of this project is to develop a machine learning (ML) co-processor that decodes brain signals using stereo electroencephalography (sEEG)—a minimally invasive, high-resolution technique—and direct brain stimulation (DiBS). By leveraging sEEG and DiBS, this BCI technology will enhance neuroplasticity in affected motor pathways and restore functional independence. This solution represents a first-of-its-kind, groundbreaking development in rehabilitative BCI technology, addressing a crucial gap for patients with motor impairments.

4. Significant achievements:

This project has achieved notable advancements across two primary areas: an EEG-based brain-computer interface (BCI) on FPGA and a low-power neural decoder SoC for BCI applications. Below is a summary of the key results.

- **EEG-Based Brain-Computer Interface (BCI) on FPGA:**

This segment of the project focused on creating an efficient signal processing architecture for real-time BCI applications. Testing on participant data from a visual attention task demonstrated that this model's accuracy is competitive with traditional BCI classification techniques, including deep learning models like EEGNet. The architecture was implemented on an FPGA platform, deploying the entire BCI processing pipeline in hardware to validate functionality.

Memory optimization was essential for meeting real-time processing demands. By exploiting sparsity in the support vector machine (SVM) model, memory requirements were reduced by **22.5 times** during training. Further optimization on the FPGA hardware used a sliding window summation algorithm, reducing memory needs by an additional **24 times**, achieving high performance with significantly lower computational and energy demands.

Additionally, a **real-time neurofeedback setup** was designed to test the system in interactive BCI scenarios. We performed an experiment where a participant successfully completed a visual attention task using the BCI system. In initial tests, participants controlled on-screen objects by shifting their visual attention, which the FPGA-based BCI processed in real time. This implementation confirms the system's suitability for neurofeedback rehabilitation and lays the groundwork for future interactive applications.

- **Low-Power Neural Decoder SoC for BCI:**

This SoC, developed for real-time neural decoding, was tested using intracortical local field potential (LFP) data from 256 electrodes implanted in a monkey performing visual tasks at Vision Lab, IISc. The software model achieved **97%** accuracy in binary classification (distinguishing human faces from objects) and **82%** accuracy in a 16-class identification task. These results demonstrate the system's capability to decode brain signals accurately, meeting the needs for high-resolution neural decoding.

The hardware system performed equivalently to its software model in simulation, verifying the design's reliability. The spike-domain processing approach, leveraging the sparsity of neural signals, enabled over **10x data compression** compared to digital systems. This significantly lowers computational requirements, reducing power consumption and extending usability.

The system's continuous-time feature extraction eliminates the need for computationally intensive FFT algorithms, achieving **minimal-latency decoding**. With low power consumption averaging around **10µW** for 10 input channels as obtained in simulation, the system scales effectively to high-density neural interfaces while adhering to power constraints.

- **List of publications:**

1. [In-review] A. Krishna, S. Debnath, A. van Schaik, M. Mehendale and C. S. Thakur, "Neural Signal Compression using RAMAN tinyML Accelerator for BCI Applications," in IEEE Transactions on Biomedical Circuits and Systems, 2024.

These achievements mark substantial progress toward a high-performance, low-latency, and energy-efficient BCI system, advancing the field of neurorehabilitation and paving the way for effective motor rehabilitation solutions for individuals with severe motor impairments.

5. Concluding remarks

The fellowship has been crucial in advancing our work on low-power, high-resolution BCI systems for individuals with severe motor impairments. Overcoming challenges in circuit design, chip tapeout complexity, and resource allocation required extensive optimization and planning. However, current funding is insufficient for the high costs associated with chip tapeouts and testing, and we are supplementing with external funds. Increased fellowship support would streamline the entire design process. Despite these challenges, the project remains on track, with promising early results showing a viable, high-accuracy, real-time neural decoding framework. Continued financial support could enable transformative rehabilitation solutions, enhancing quality of life and independence for individuals with neurological disorders.